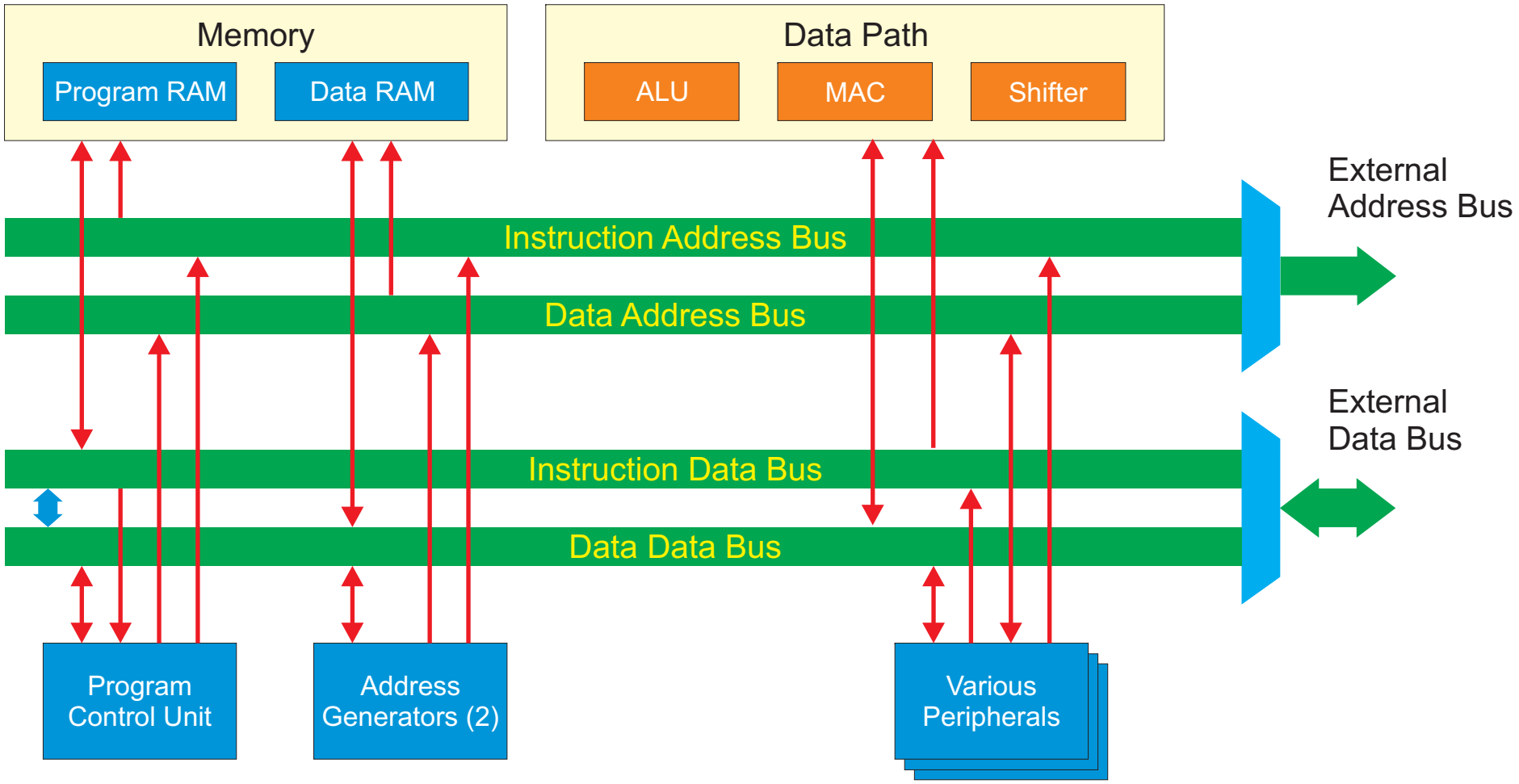
Example: Analog Devices ADSP-21xx DSP Architecture



Example: FIR Filter Optimization on the Texas Instruments TMS320C62xx

Before

```
Loop:
          LDW.D2     *B4++,B2    ; load coeff[ 0 ] and coeff[ 1 ]
 ||       LDW.D1     *A7--,A2    ; load state[ 0 ] and state[ 1 ]
          NOP        4           ; wait for loads to finish
          MPYHL.M1X  A2,B2,A3    ; p0[ i ] = coeff[ 2i   ] * state[ 2i   ]
 ||       MPYLH.M2X  A2,B2,B7    ; p1[ i ] = coeff[ 2i+1 ] * state[ 2i+1 ]
 ||       ADD.S2     -1,B0,B0    ; decrement loop counter
          NOP        1           ; wait for multiplications to finish
          ADD.L1     A0,A3,A0    ; sum0 += p0[ i-2 ]
 ||       ADD.L2     B1,B7,B1    ; sum1 += p1[ i-2 ]
 || [B0]  B.S1       Loop        ; conditional branch to Loop
          NOP        5           ; wait for branch to take effect
```

Speed: 6.5 instruction cycles per tap. That's very slow for a DSP Processor!

After

```
          ADD.L1     A0,A3,A0    ; sum0 += p0[ i-2 ]
 ||       ADD.L2     B1,B7,B1    ; sum1 += p1[ i-2 ]
 ||       MPYHL.M1X  A2,B2,A3    ; p0[ i ] = coeff[ 2i   ] * state[ 2i   ]
 ||       MPYLH.M2X  A2,B2,B7    ; p1[ i ] = coeff[ 2i+1 ] * state[ 2i+1 ]
 ||       LDW.D2     *B4++,B2    ; load coeff[ 2i+10 ] and coeff[ 2i+11 ]
 ||       LDW.D1     *A7--,A2    ; load state[ 2i+10 ] and state[ 2i+11 ]
 || [B0]  ADD.S2     -1,B0,B0    ; conditional decrement loop counter
 || [B0]  B.S1       Loop        ; conditional branch to Loop
```

Speed: 0.5 instruction cycles per tap. That's the best a 'C62xx can do.

Not shown: about 24 instructions to prime the software pipeline and start the loop, and 3 instructions for final calculations.